IN THE CLAIMS

Presented below is a complete listing of all the claims in the format as permitted by the PTO waiver of 37 CFR 1.121 in accordance with the Official Gazette Notice of February 25, 2003.

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19. (Currently Amended) A memory device, comprising memory storage and three different interfaces to operate the memory storage ~~device~~ in at least one of three different modes, wherein the memory storage and the three different interfaces reside in a common die.

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20. (Previously Amended) The memory device of claim 21, further comprising selection circuitry to select among the plurality of different interfaces.

21. (Previously Amended) The memory device of claim 19, wherein the three different interfaces comprise:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

22. (Original) The memory device of claim 21, wherein the memory device is a flash memory and the test interface is a standard flash memory interface.

23. (Original) The memory device of claim 21, wherein the operation interface is a proprietary interface.

24. (Previously Amended) The memory device of claim 20, wherein the selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

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25. (Currently Amended) The memory device of claim 24, wherein the three different interfaces ~~comprises~~ comprise:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

26. (Currently Amended) A component board, comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising memory storage and three different interfaces to operate the memory storage ~~device~~ in at least one of three different modes, where in the memory storage and the three different interfaces reside in a common die.

27. (Previously Amended) The component board of claim 26, further comprising selection circuitry to select among the three different interfaces.

28. (Previously Amended) The component board of claim 27, wherein the selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

29. (Previously Amended) The component board of claim 26, wherein the three different interfaces comprise:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

30. (Original) The component board of claim 29, wherein the memory device is a flash memory, the test interface is a standard flash memory interface, and the operation interface is a proprietary interface.

31. (Original) The component board of claim 27, wherein the memory device is a BIOS memory.

32. (Currently Amended) A computer system, comprising:

a peripheral device; and

a system board coupled to the peripheral device, the system board comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising memory storage and three different interfaces to operate the memory storage ~~device~~ in at least one of three different modes, where in the memory storage and the three different interfaces reside in a common die.

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33. (Previously Amended) The computer system of claim 32, further comprising selection circuitry to select among the three different interfaces.

34. (Previously Amended) The computer system of claim 33, wherein the selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

35. (Previously Amended) The computer system of claim 32, wherein the three different interfaces comprise:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

36. (Original) The computer system of claim 35, wherein the memory device is a flash memory and the test interface is a standard flash memory interface and the operation interface is a proprietary interface.

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37. (Original) The computer system of claim 33, wherein the memory device is a BIOS memory.

38. (Original) A memory device, comprising a plurality of different interfaces to operate the memory device in a plurality of different modes, wherein the memory device is a flash memory and wherein one of the plurality of interfaces is a standard flash memory interface.

39. (Currently Amended) A method, comprising:

selecting an interface from among at least a programming interface and a test interface in a memory device having memory storage, wherein the programming interface, the test interface ~~reside~~ and the memory storage reside in a common die, the programming interface to program the memory storage and the test interface to test the memory storage; and

operating the memory device with the selected interface.

40. (Original) The method of claim 39, wherein selecting comprises selecting the programming interface and wherein operating comprises programming the memory device with code using the programming interface.

41. (Original) The method of claim 39, wherein selecting comprises selecting the test interface and wherein operating comprises testing the memory device for defects using the test interface.